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PATENT APPLICATION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:
Inventors: **Dong-Ho KIM et al.**
For: **SEMICONDUCTOR MANUFACTURING APPARATUS FOR PHOTOLITHOGRAPHIC PROCESS**
Enclosures:
[X] Specification (pages 1-6); claims (pages 7-8); abstract (page 9)
[X] 6 sheet(s) of formal drawings
[X] Executed Combined Declaration and Power of Attorney
[X] Executed Assignment
[X] Korean Priority Document #99-55236 filed December 6, 1999
[X] Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

CLAIMS AS FILED				
For	Number Filed	Number Extra	Rate	Basic Fee $690
Total Claims	7-20	0	x $ 18 =	$0
Independent Claims	1-3	0	x $ 78 =	$0
TOTAL FILING FEE				$690

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM P.C.

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM P.C.
1030 S.W. Morrison Street Portland OR 97205 (503) 222-3613

SEMICONDUCTOR MANUFACTURING APPARATUS FOR PHOTOLITHOGRAPHIC PROCESS

This application relies for priority upon Korean Patent Application No. 1999-55236, filed on December 6, 1999, the contents of which are herein incorporated by reference in their entirety.

Field of the Invention

The present invention relates to a semiconductor manufacturing device and, more particularly, to a semiconductor manufacturing apparatus for a photolithographic process including a coating process and a developing process.

Background of the Invention

A variety of steps are applied to a semiconductor manufacturing process, forming an electric circuit on a substrate such as a semiconductor substrate, a glass substrate, and a liquid crystal panel. Photolithography is classified into a coating process, an exposure process, and a developing process. In the coating process, a photoresist (PR) is conformally coated on a surface of the substrate. Light passes a circuit pattern drawn on a mask using a stepper, exposing the circuit pattern to the substrate on which a photoresist layer is formed, in the exposure process. A layer of a light-receiving portion is developed in the developing process.

Figs. 1-2 schematically illustrate one and another example of a conventional semiconductor manufacturing apparatus for a photolithographic process, respectively.

Referring now to Fig. 1, a semiconductor manufacturing apparatus 200 for a photolithographic process includes a port 210 where a substrate is loaded/unloaded, a spin coater (SCW) 220 for coating a photoresist onto the substrate, a spin developer (SDW) 230 for developing the substrate, a bake unit (BAKE) 240 for heating up the substrate, a wide expose edge wafer (WEEW) 250 for exposing unnecessary photoresist around a circumference of the substrate. The foregoing units are horizontally arranged according to process flow, and divided at both sides of a central path 260. A robot 270, placed in the path 260, carries the substrate to the port 210, an interface 280, or each of the process units. The interface 280 is a port where an exposure system 150 and the substrate comes in and goes out.

Referring now to Fig. 2, similar to the apparatus 200, a semiconductor manufacturing apparatus 300 includes a port 310, a spin coater (SCW) 320, a spin developer (SDW) 330, a bake unit (BAKE) 340, and a wide expose edge wafer (WEEW) 350. The foregoing units are

divided at both sides of central paths 360 and 380. To increase operating ratio in comparison with the apparatus 200, the semiconductor manufacturing apparatus 300 utilizes two robots 370 and 390 as a carrier for carrying a substrate. Units for a coating process and units for a developing process are horizontally arranged. A robot is arranged in the coating units and developing units, respectively. A first interface 400 is arranged therebetween. A robot 370 of a coating process region carries a substrate to the port 310, the first interface 400, or each process unit of the coating process region. A robot 390 of a developing process region carries the substrate to the first interface 400, the second interface 410, or each process unit of the developing process. The second interface 410 is a port where the exposure system 150 and the substrate come in and go out.

Technologies related to the foregoing semiconductor manufacturing apparatus are disclosed in U. S. Patent No. 5,399,531, issued by Wu.

Increasing the operating ratio is subject to limitation. In the semiconductor manufacturing apparatus 200 and 300, a coated substrate is carried to an exposure system and, thereafter, the substrate exposed in the exposure system is developed and outwardly carried. Based upon proceeding order of the photolithography, a substrate can sequentially be carried. If a process of one unit is stagnated, a process of others can be stagnated to drop the operating ratio. If only one specific process (e.g., developing process) requires performing, the operating ratio can also be dropped because other units should be carried through a path where they are arranged. Adding each of the units to the apparatus 300 shown in Fig. 2 from the apparatus 200 shown in Fig. 1 causes increase in an equipment area. This cannot achieve practical increase in the operating ratio. Merely, processing units are increased to raise the operating ratio.

Summary of the Invention

It is therefore an object of the invention to provide a semiconductor manufacturing apparatus for a photolithographic process, which can maximize an operating ratio of equipment.

It is another object of the invention to provide a semiconductor manufacturing apparatus for a photolithographic process, which can be installed with a relatively small area and easily apply a new process.

According to the invention, a semiconductor manufacturing apparatus for a photolithographic process having a coating process and a developing process includes a first port, a second port, a coating unit, and a developing unit. In the first and second ports, a

substrate comes in and goes out. There is a constant distance between the first and second substrates. The coating unit is installed to couple the first port to the second port, carry the substrate therebetween, and perform a coating process. The developing unit is opposite to the coating module to couple the first port to the second port, carry the substrate therebetween, and perform a developing operation.

The coating unit is composed of: a first path for coupling the first port to the second port; a coating module installed along one side of the first path; and a first carrier, moving between the first and the second ports through the first path, for carrying the substrate to the first port, the second port, or the coating module. The developing unit is composed of: a second path for coupling the first port to the second port; a developing module installed along one side of the second path; and a second carrier, moving therebetween through the second path, for carrying the substrate to the first port or the second port or the developing module. In this case, the coating module includes a coater arranged at one side of the first path and a bake unit arranged at the other. The developing module includes a developer arranged at one side of the second path and a bake unit arranged at the other. The bake unit includes at least one heating plate for heating up the substrate and at least one cooling plate for cooling down the heated substrate.

The semiconductor manufacturing apparatus for a photolithographic process is coupled to an exposure system.

The coating unit and the developing unit are isolated from each other by an intermediate wall. The apparatus further includes an air-conditioning apparatus, installed at the intermediate wall, for removing particles created in the coating unit and the developing unit.

The coating process and the developing process are separately performed to scarcely cause process stagnation. In particular, it is possible to efficiently remove stagnation caused by carrying the substrate. Making the most use of the units is to create a stable operating ratio of equipment. The units are stacked, thereby reducing an installation area and easily applying a new or additional process.

A further understanding of the nature and advantage of the invention herein may be realized by reference to the remaining portions of the specification and the attached drawings.

Brief Description of the Drawings

Fig. 1 is a block diagram for illustrating one example of a semiconductor manufacturing apparatus for a photolithographic process in accordance with a prior art;

Fig. 2 is a block diagram for illustrating another example of a semiconductor manufacturing apparatus for a photolithographic process in accordance with a prior art;

Fig. 3 is a block diagram for illustrating a semiconductor manufacturing apparatus in accordance with the invention;

Fig. 4 is a top plan view of a semiconductor manufacturing apparatus shown in Fig. 3;

Fig. 5 is a bottom view of a semiconductor manufacturing apparatus shown in Fig. 3; and

Fig. 6 is a perspective view for schematically showing one example of a bake unit applied to a semiconductor manufacturing apparatus shown in Fig. 3.

Description of the Preferred Embodiment

Now, the present invention will be described more fully hereinafter with reference to attached drawings wherein the same numerals denote the same components.

Referring now to Figs. 3-5, a semiconductor manufacturing apparatus 10 includes a coating module 40 which is composed of units for carrying out a developing process, and a developing module 70 which is composed of units for carrying out a developing process. In this embodiment, the coating module 40 is arranged on an upper layer and the developing module 70 is arranged on a lower layer. Moreover, it is naturally possible that the coating module 40 is arranged on the lower layer and the developing module 70 is arranged on the upper layer. A multi-layer (more than two layers) structure may be applied. A path and a carrier for carrying a substrate are separately made to separately perform the coating process and the developing process. That is, a first path 60 for carrying the substrate through the coating module 40 is arranged along the coating module 40, and a second path 80 for carrying the substrate through the developing module 70 is arranged along the developing module 70. A variety of types may be applied to the arrangements of the coating module 40 to the first path 60, and of the developing module 70 to the second path 80. In this embodiment, the coating module 40 is arranged at both sides of the first path 60 and the developing module 70 is arranged at both sides of the second path 80. The upper layer and lower layers are isolated from each other by an intermediate wall 100, which is generally an interlayer wall. An air-conditioning apparatus for removing particles created in the upper layer and/or the lower layer may be installed at the intermediate wall 100. Because technology for installing the air-conditioning apparatus is well-known by those skilled in the art, description thereof will be skipped herein. A first robot 62, which is located at the first path 60, serves as a carrier for carrying the substrate by moving along the first path 60. A

second robot 82, which is located at the second path 80, serves as a carrier for carrying the substrate by moving along the second path 80. The semiconductor manufacturing apparatus 10 can freely carry the substrate to the port 20 where the substrate is loaded/unloaded, and between the exposure system 150 and the interface 30.

Referring to Figs. 3-5 again, the semiconductor manufacturing apparatus 10 has two ports where a substrate comes in and goes out. One is a port 20 where the apparatus 10 carries out a photolithographic process or a specific process. The other is an interface 30 having a constant distance from the port 20. A port driver 22 is installed in the port 20 and an interface driver 32 is installed in the interface 30, smoothly carrying the substrate. The port driver 22 and the interface driver 32 correspond to both a robot of the upper layer and that of the lower layer or correspond to the robots, respectively. In this embodiment, the port 20 and the interface 30 can carry both a substrate of the upper layer and that of the lower layer using one driver 22 and 32, respectively. Naturally, those skilled in the art can apply a variety of types thereof.

The coating module 40, the first path 60, and the first robot 62, which couple the port 20 to the interface 30, serve as a coating unit for carrying the substrate therebetween and performing a coating process. The developing module 70, the second path 80, and the second robot 82, which are stacked on the coating unit in line and couple the port 20 to the interface 30, serve as a developing unit for carrying the substrate therebetween and performing a developing process.

Conventionally, although only a developing process requires carrying out, a substrate should be carried through a region of a coating process. This invention solves such a problem, maximizing efficiency of the process.

Referring now to Figs. 4-6, the semiconductor manufacturing apparatus 10 has the above-described architecture wherein units composing the coating module 40 are arranged at both sides of the first path 60 and unit composing the developing module 70 are arranged at both sides of the second path 80. In the coating module 40, as shown in Fig. 4, a bake unit 50 is installed at one side of the first path 60 and a coater 42 is installed at the other. In the developing module 70, as shown in Fig. 5, the bake unit 50 is installed at one side of the second path 80 and a developer 72 is installed at the other. The composing units of the modules 40 and 70 can be controlled by a size of the substrate. Various diameters such as 6, 8, 12, 15, and 15 inches have been applied to a wafer, and a size thereof is steadily growing. Therefore, it is necessary to consider a substrate applied to the coating module 40 and the developing module 70.

According to the semiconductor manufacturing apparatus 10 of this invention, an installation area can be reduced and a unit for a new process can easily be applied without variation of other units therein. The bake unit 50 is equipped with a heating plate (H/P) 52 for heating up a substrate and a plurality of cooling plates (C/P) 54 for cooling the heated substrate. The heating and cooling plates 52 and 54 are alternatively stacked (see Fig. 5) or are stacked in a pair (see Figs. 6-7). For example, a type thereof is two-row and two-step or two-row and five-step.

As so far described, a coating process and a developing process are separately performed to prevent process stagnation. Particularly, stagnation caused by carrying a substrate can efficiently be prevented. Further, the coating process and developing process are separately performed to make the most use of each unit, so that it is possible to stably maintain an operation ratio of equipment. Because each unit is stacked, it can be installed in a relatively small area and a new or additional process can easily be applied.

While particular embodiment of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspect and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.

WHAT IS CLAIMED IS:

1. A semiconductor manufacturing apparatus for a photolithographic process including a coating process and a developing process, the apparatus comprising:

a first port where a substrate comes in and goes out;

a second port, having a constant distance from the first port, where the substrate comes in and goes out;

coating means, coupling the first port to the second port, for carrying the substrate between the first port and the second port and performing the coating process; and

developing means, coupling the first port to the second port, for carrying the substrate between the first port and the second port and performing the developing process, the developing means being stacked on the coating means in line.

2. The apparatus of Claim 1, wherein the coating means includes:

a first path which couples the first port to the second port;

a coating module which is arranged along one side of the first path; and

a first carrier, which moves between the first port and the second port, for carrying a substrate to the first port or the second port or the coating module,

wherein the developing means includes:

a second path which couples the first port to the second port;

a developing module which is arranged along one side of the second path; and

a second carrier, which moves between the first port and the second port, for carrying the substrate to the first port or the second port or the developing module.

3. The apparatus of Claim 1, wherein the second port is coupled to an exposure system.

4. The apparatus of Claim 1, wherein the coating means and the developing means are isolated from each other by an intermediate wall.

5. The apparatus of Claim 2, wherein the coating module includes:

a coater which is arranged at one side of the first path; and

a bake unit which is arranged at the other side of the first path and opposite to the coater, and

wherein the developing module includes:

a developer which is arranged at one side of the second path; and

a bake unit which is arranged at the other side of the second path and opposite to the developer.

6. The apparatus of Claim 4 further comprising an air-conditioning apparatus, which is installed at the intermediate wall, for removing particles created in the coating means and the developing means.

7. The apparatus of Claim 5, wherein the bake unit includes:

at least one heating plate for heating up a substrate; and

at least one cooling plate for cooling down the heated substrate.

Abstract of the Disclosure

A semiconductor manufacturing apparatus for a photolithographic process having a coating process and a developing process is described, which includes a first port, a second port, a coating member, and a developing member. The first port and second port have a constant distance from each other, where a substrate comes in and goes out. The coating member, which couples the first port to the second port, carries the substrate between the first port and the second port and carries out the coating process. The developing member, which couples the first port to the second port and is stacked on the coating member, carries the substrate therebetween and carries out the developing process. The apparatus can stably maintain an operating ratio of equipment, and be installed in a relatively small area.

Fig. 1

(Prior Art)

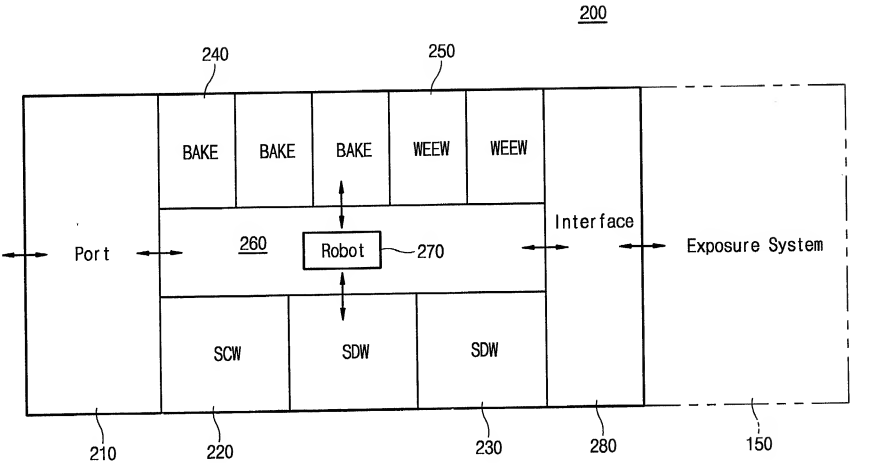


Fig. 2

(Prior Art)

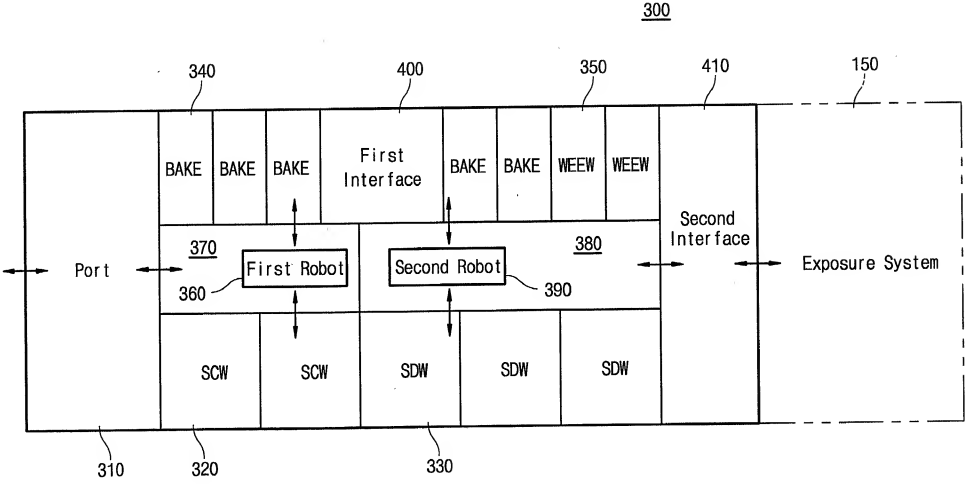


Fig. 3

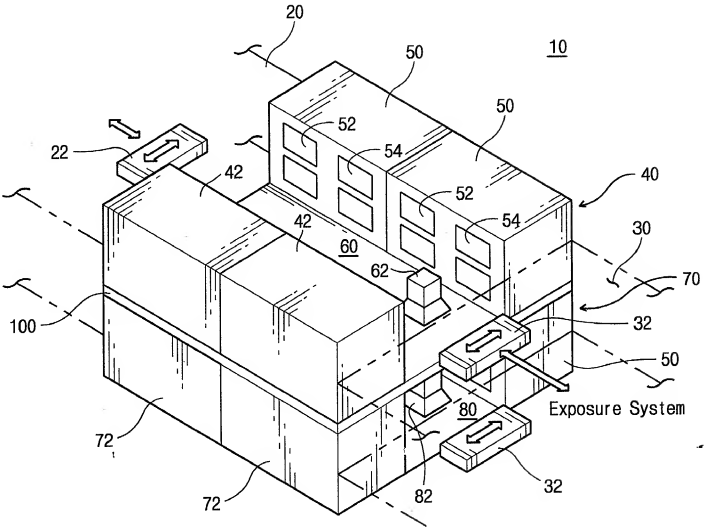


Fig. 4

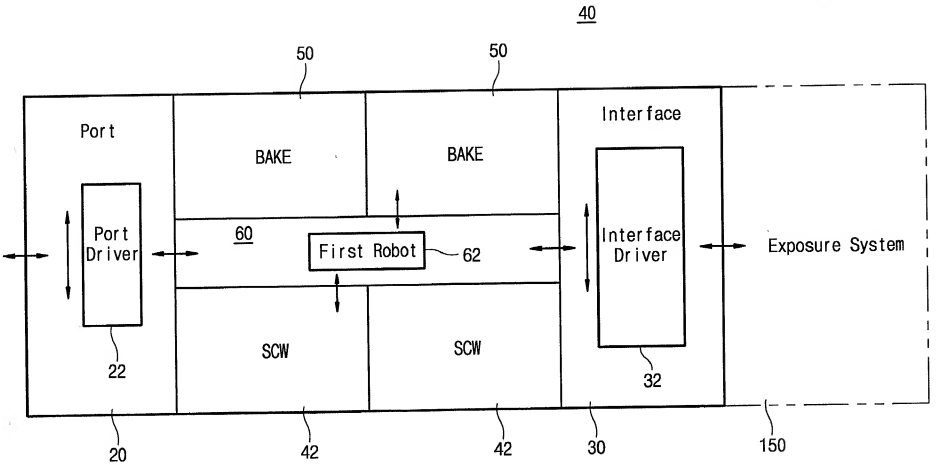


Fig. 5

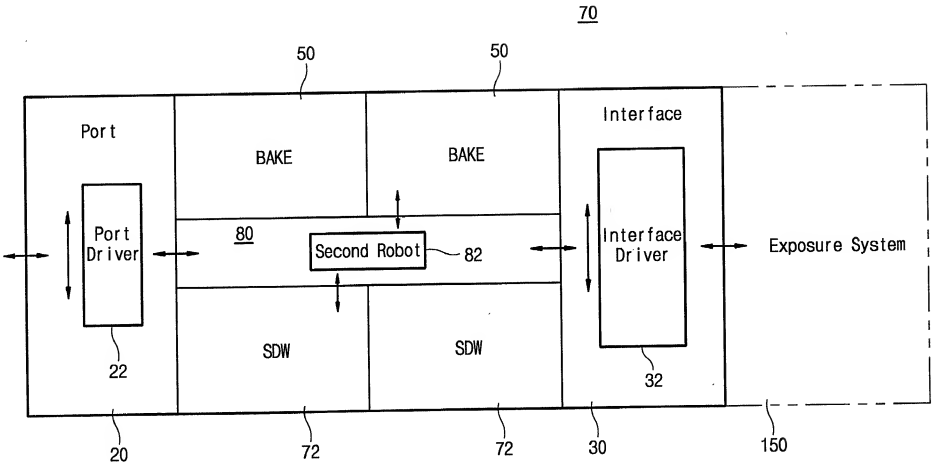
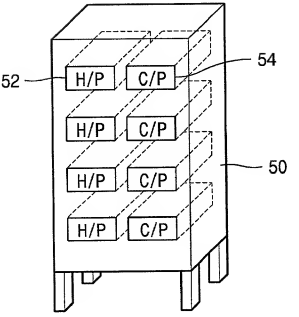


Fig. 6



PATENT APPLICATION
Attorney Docket No.

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **SEMICONDUCTOR MANUFACTURING APPARATUS FOR PHOTOLITHOGRAPHIC PROCESS**, the specification of which:

[X] is attached hereto.
[ ] was filed on _____ as Application No. _____
[ ] and was amended on _____(if applicable)
[ ] with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?	
99-55236	Republic of Korea	6 December 1999	[X]	[ ]
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No.	Filing Date

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the

prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

______________ ______________ ______________

(Application No.) (Filing Date) (Status) (patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Customer No. 20575

Attorney Name	Registration No.
Jerome S. Marger	26,480
Alexander C. Johnson, Jr.	29,396
Alan T. McCollom	28,881
James G. Stewart	32,496
Glenn C. Brown	34,555
Stephen S. Ford	35,139
Gregory T. Kavounas	37,862
Scott A. Schaffer	38,610
Joseph S. Makuch	39,286
James E. Harris	40,013
Graciela G. Cowger	42,444
Ariel Rogson	43,054
Craig R. Rogers	43,888

Direct all telephone calls to at (503) 222-3613 and send all correspondence to:

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, Oregon 97205

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Dong-Ho KIM

Inventor's signature: Dong-Ho KIM 2000.9.7 (Date)

Residence: Chonan-shi, Chungcheongnam-do, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 623-5, Upsung-dong, Chonan-shi, Chungcheongnam-do, Republic of Korea

Full name of second inventor: Hee-Young KANG

Inventor's signature: HEE-YOUNG KANG 2000. 9. 9 (Date)

Residence: Chonan-shi, Chungcheongnam-do, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 623-5, Upsung-dong, Chonan-shi, Chungcheongnam-do, Republic of Korea

Full name of third inventor: Ki-Sung CHO

Inventor's signature: CHO-KI SUNG 2000 9.9 (Date)

Residence: Chonan-shi, Chungcheongnam-do, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 623-5, Upsung-dong, Chonan-shi, Chungcheongnam-do, Republic of Korea